WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a dummy pattern for alleviating for a difference in density in an arranged pattern;

a power-supply wire; and

a ground wire;

wherein said dummy pattern is electrically connected to a reference wire which is either said power-supply wire or said ground wire.

2. The semiconductor device according to claim 1, wherein electrical connection between said dummy pattern and said reference wire is made through paths formed by a process including a first step of:

setting all said dummy patterns as unconnected dummy patterns, and a second step of:

retrieving any said unconnected dummy patterns that overlap each other and are adjacent to each other in an up and down direction with not less than a predetermined distance using a target wire which is either said reference wire or wires having the same electrical potential as said reference wire as the starting point,

in the case when, as a result of said retrieval, any of such said unconnected dummy patterns are detected, recognizing these as adjacent dummy patterns and providing an interlayer connection between said target wire and said adjacent dummy patterns, as well as changing the setting of said adjacent dummy patterns as non-unconnected dummy patterns with said adjacent dummy patterns being set as those having the same electric potential as said target wire,

recursively repeating said second step with respect to all said reference wires and those wires having the same electrical potential as said reference wire,

in place of said reference wire, with the other of said power-supply wire and said ground wire being newly used as a reference wire, recursively repeating said second step with respect to all said reference wires and those

wires having the same electrical potential as said reference wire.

3. A designing method of a semiconductor device which is a method for generating dummy patterns so as to eliminate a difference in density in a wiring pattern based upon wiring layout information that has been provided, and for electrically connecting said dummy patterns and said reference wire with one of a power-supply wire and a ground wire being used as a reference wire based upon layout information of power-supply wire and ground wire that have been supplied, is provided with a process including a first step of:

setting all said dummy patterns as unconnected dummy patterns, and a second step of:

retrieving any said unconnected dummy patterns that overlap each other and are adjacent to each other in an up and down direction with not less than a predetermined distance using a target wire which is either said reference wire or wires having the same electrical potential as said reference wire as the starting point,

in said case when, as a result of said retrieval, any of such said unconnected dummy patterns are detected, recognizing these as adjacent dummy patterns and providing an interlayer connection between said target wire and said adjacent dummy patterns, as well as changing the setting of said adjacent dummy patterns as non-unconnected dummy patterns with said adjacent dummy patterns being set as those having the same electric potential as said target wire,

recursively repeating said second step with respect to all said reference wires and those wires having the same electrical potential as said reference wire,

in place of said reference wire, with the other of said power-supply wire and said ground wire being newly used as said reference wire, recursively repeating said second step with respect to all said reference wires and those wires having the same electrical potential as said reference wire; thus, connection path information on each of dummy patterns and either of said power-supply wire and said ground wire is directed.

4. A designing method of a semiconductor device comprising steps of:

carrying out the designing method of a semiconductor device according to claim 3, after a layout designing job, and

executing a design rule check, a coincident inspection between a circuit diagram and a layout, and calculations on capacitance and resistance of wiring.

5. A designing device of a semiconductor device comprising:

a dummy pattern generation means for generating dummy patterns so as to eliminate a difference in density in a wiring pattern based upon wiring layout information that has been provided;

an unconnected dummy pattern setting means for setting all said dummy patterns as unconnected dummy patterns so as to electrically connect said dummy patterns and said reference wire with one of a power-supply wire and a ground wire being used as a reference wire based upon layout information of a power-supply wire and a ground wire that has been supplied;

a first recursive process executing means which retrieves any said unconnected dummy patterns that overlap each other and are adjacent to each other in an up and down direction with not less than a predetermined distance using a target wire which is either said reference wire or wires having the same electrical potential as said reference wire as the starting point for a dummy pattern connection process,

which in said case when, as a result of said retrieval, any of such unconnected dummy patterns are detected, recognizes these as adjacent dummy patterns and provides an interlayer connection between said target wire and said adjacent dummy patterns, as well as changing the setting of said adjacent dummy patterns as non-unconnected dummy patterns with said adjacent dummy patterns being set as those having said same electric potential as said target wire,

which recursively repeats said sequence of jobs with respect to all said reference wire and those wires having the same electrical potential as

said reference wire, and

a second recursive process job executing means which, in place of said reference wire, with the other of said power-supply wire and said ground wire being newly used as said reference wire, recursively repeats said dummy pattern connection process with respect to all said reference wires and those wires having said same electrical potential as said reference wire.